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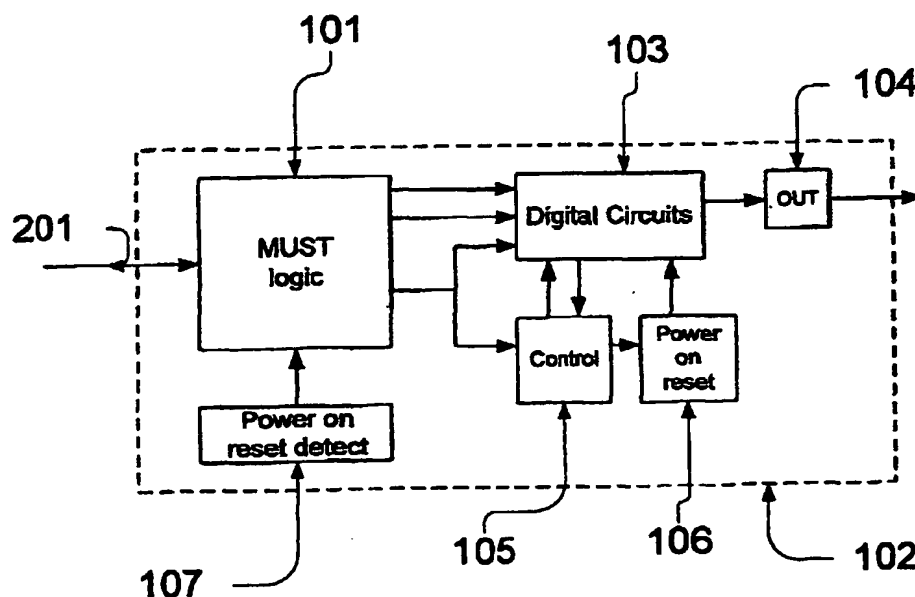
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(54) Title: SINGLE PIN MULTILEVEL INTEGRATED CIRCUIT TEST INTERFACE



(57) Abstract: An integrated circuit (102) comprises one or more integrated circuit elements which may interact with other circuitry via one or more input/output pins. In the present invention the circuit elements include and interface element (101) for interfacing with external test circuitry. The interface element communicates with the external test circuitry via a single input/output pin (201) dedicated for testing.



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# INTERNATIONAL SEARCH REPORT

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PCT/03/02380

**A. CLASSIFICATION OF SUBJECT MATTER**  
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According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X	PATENT ABSTRACTS OF JAPAN vol. 006, no. 230 (E-142), 16 November 1982 (1982-11-16) -& JP 57 133656 A (NIPPON DENKI KK), 18 August 1982 (1982-08-18) abstract ---	1-3,5
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 516 (P-1443), 23 October 1992 (1992-10-23) -& JP 04 191683 A (MITSUBISHI ELECTRIC CORP), 9 July 1992 (1992-07-09) abstract --- -/-	1,2

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☒ Patent family members are listed in annex.

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## C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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